VOID FORMATION: EMERGING ISSUES IN MATERIALS COMPATIBILITY AND RELIABILITY OF PB-FREE ASSEMBLIES

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Abstract: With the RoHS Deadline now past and Pb-free manufacturing having become a reality, more complex issues than choice of alloy continue to emerge, particularly regarding materials compatibility and reliability. We examine the root causes of some of these issues, particularly void formation during high temperature annealing, drop/shock response of Pb-free assemblies, and fillet lifting. In addition, we will review some of the fundamental materials properties that affect backward compatibility for applications that are exempt from RoHS and WEEE.

1. INTRODUCTION

With the RoHS and WEEE deadline of July 1, 2006 approached, microelectronic companies worldwide began to convert their production lines to Pb-free assembly. As the number of companies manufacturing with Pb-free increased, the list of implementation issues has grown due to the number of and variability in assembly materials and processes examined. These issues require an examination of materials and processes that we previously took for granted, in order to understand their root causes and to develop solutions for Pb-free implementation.

Early Pb-free research focused on the choice of a new "standard" solder alloy to replace Sn-Pb eutectic based on manufacturing and reliability trials, primarily using accelerated thermal cycling (ATC) in comparison with Pb-Sn and reactions with common surface finishes to identify the best alloys.[1-6] The current generation of Pb-free research is examining an extremely wide range of issues, including

- developing the relationship between field performance under different conditions and ATC testing for different ATC profiles [7,8] and
- understanding the reasons for the observed shock/drop and vibration behaviour of different combinations of solder alloys, components, and surface finishes, [9-11]

In this paper we examine the possible root cause of one such issue for Pb-free alloys: the void formation sometimes observed between electroplated copper and Sn-containing alloys during high temperature annealing (100°C-160°C). [9-17] After soldering with either Sn-Pb eutectic solder or Pb-free solders and during subsequent annealing of the resulting assemblies, voids have been observed to sometimes form in the Cu_3Sn and along the Cu-Cu_3Sn interface. The amount of voiding can range from zero to the extreme case where the Cu-Cu_3Sn interface has disintegrated. Understanding the conditions for void formation and the effect of voids on drop/shock behaviour are the subjects of serious concern.

2. VOID FORMATION DURING ANNEALING OF SOLDER JOINTS

An illustration of the observed variability in void formation is in the work of Borgesen et al., [14] where the tendency for void formation differed by circuit board manufacturer and sometimes exhibited the extremes cases for different board lots from a single manufacturer. Examples of the extremes in void formation are seen in the cross-sections from Borgesen (Figure 1).

Early work by Yang and Messler in 1994 [12] suggested that the tendency for void formation is determined by the characteristics of the electrodeposited copper. They found that rolled copper annealed up to 12 days at 190 °C in contact with Sn-Ag eutectic solder showed no void formation while an electrodeposited copper showed void formation after three days at 190 °C. Yang and Messler conjectured that the observed void formation was a result of the "Kirkendall effect," caused by unequal diffusion of Sn and Cu

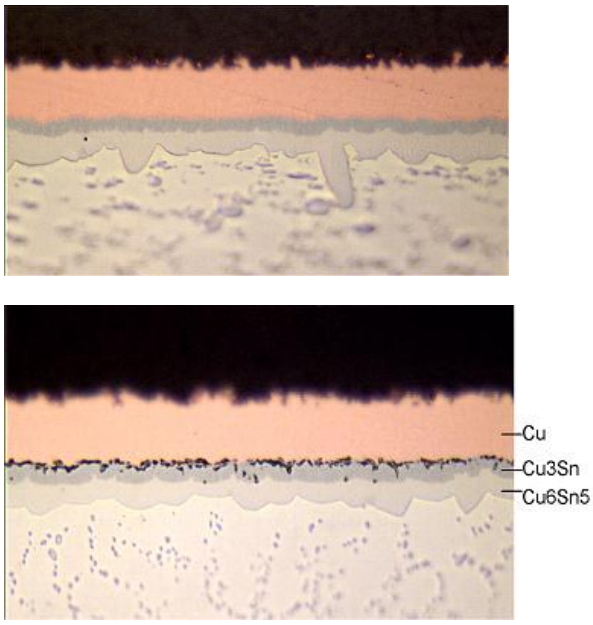


Figure 1. Interfaces between Sn-Ag-Cu solder balls (at bottom), intermetallic layers, and electroplated Cu pads on identically aged samples (1000 hours @ 150°C). Copper samples were produced from two plating lots, but were assembled using the same solder ball lot, the same flux lot, and in the same oven on the same day using the same reflow conditions (atmosphere, thermal profile). The test samples were thermally aged at the same time in the same oven. (reproduced from Borgesen, [15, 16]]

and accelerated by hydrogen incorporated into the lattice during electrodeposition. Subsequent researchers have attributed the observed void formation to the Kirkendall effect alone. This role of the Kirkendall effect in void formation is not supported by the theory behind the Kirkendall effect and diffusion studies in Cu-Sn.

2.1 Analysis of Kirkendall Effect in Cu-Sn

The simplest example for understanding the Kirkendall effect is interdiffusion of two elemental metals forming a single phase solid solution. Unequal volume diffusion of two species on a single lattice leads to unequal mass transfer across the initial interface. When inert markers are placed at the initial interface between the two materials, the markers move during diffusion towards region where the faster diffusing elements originated.. As a result of this net mass flow, compressive stresses may be created in the region where the faster diffusing element is moving. As a result of vacancy formation, migration, and deposition, voids may form in the region where the faster diffusing element originated.. It should be remembered that porosity formation is

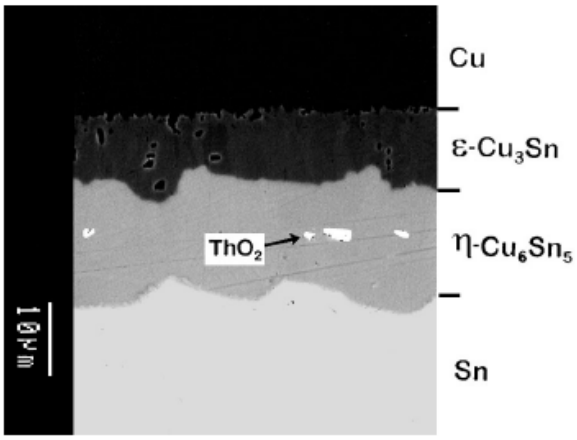


Figure 2. Backscattered electron image (BEI) of intermetallics formation in the diffusion zone between Cu and Sn after 225 h in vacuum at 215 °C. Thoria particles indicated by arrow were used as inert marker. (reproduced from Paul, [19, 20])

not necessary for the Kirkendall effect to operate. If porosity does form, however, the markers should appear to move toward the source of the faster diffusing element and the porosity should appear in the same region. [18]

Diffusion between Cu and Sn is significantly more complicated than a simple *single phase*, binary diffusion couple. When Cu is in contact with Sn and Sn-containing alloys at typical temperatures where voids are seen (100 °C – 160 °C), interdiffusion leads to the formation of two intermetallic phases (Cu_3Sn and Cu_6Sn_5). With four different phases with different crystal structures, there are four regions in which diffusion between Cu and Sn may occur with different Kirkendall effects in each phase. Preliminary experiments by Paul et al. at 215 °C suggest that the greatest difference between Cu and Sn diffusion in the intermetallics at that temperature exists in the Cu_6Sn_5 phase, with Sn having a diffusivity 1.6 times the diffusivity of Cu in that phase. Voids are therefore predicted to form towards the Sn-Cu_6Sn_5 interface. [19, 20] Void formation at that location has never been observed.

Another explanation must be sought. The Kirkendall effect is not expected to be a process that can be turned on or off depending on the plating lot, unless additional diffusing species or internal stresses are involved. It should occur reproducibly with the same end members of the diffusion couple under the same diffusion conditions and the porosity should form in the same region towards which the inert markers move.

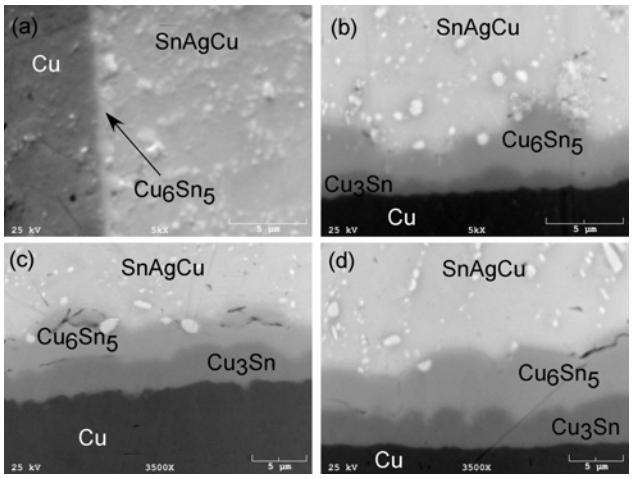


Figure 3 SEM images taken in BEI mode (except image (a) – secondary electron image) showing the formation of two IMC layers in the SnAgCu-dipped high purity Cu with increased annealing time at 150°C for (a) 0 days – control, (b) 5 days, (c) 25 days, and (d) 40 days. The white phase in the SnAgCu solder is Ag_3Sn. No voids were observed.

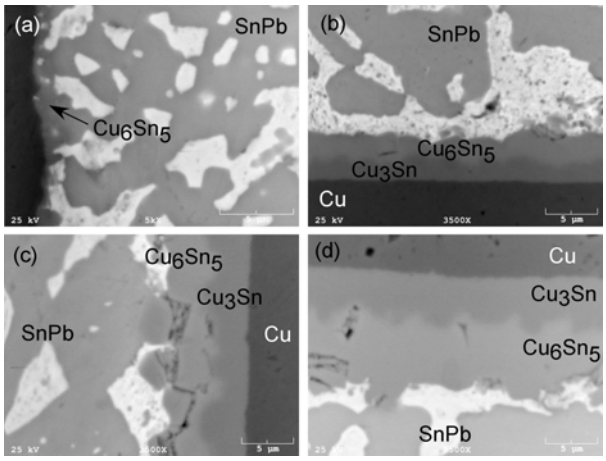
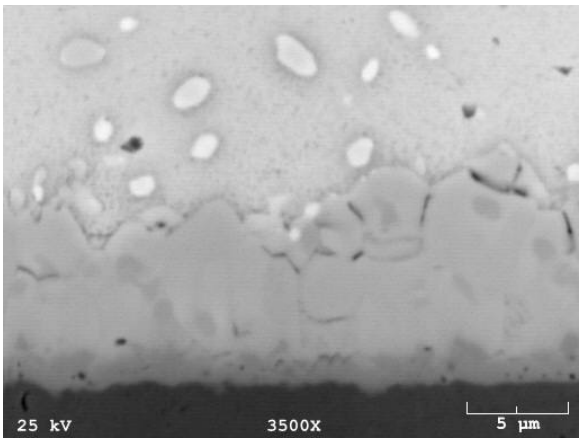


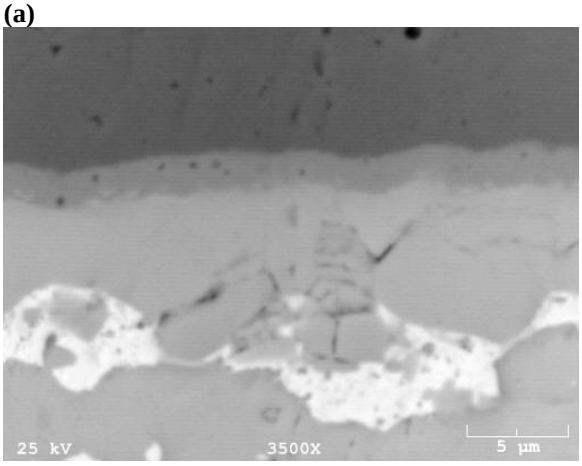
Figure 4 SEM images taken in BEI mode showing the formation of two IMC layers in the SnPb-dipped high purity Cu strips with increased annealing at 150°C for (a) 0 days – control, (b) 5 days, (c) 25 days, and (d) 40 days. The white phase in the SnPb solder is lead. No voids were observed.

2.2 No Void Formation Observed in Annealed High-Purity Copper - Solder Samples

Base-line experiments for void formation in high-purity copper in contact with tin-silver-copper and eutectic Sn-Pb were performed at 125°C and 150°C as a function of time. Thin copper sheet samples (99.999% pure, Alfa Aesar) were dip coated with Sn-3.0Ag-0.5Cu (wt%) lead-free solder or SnPb eutectic solder (37 wt% Pb) using a non-activated rosin flux and a solder pot temperature of 245°C± 5°C and



(a)



(b)

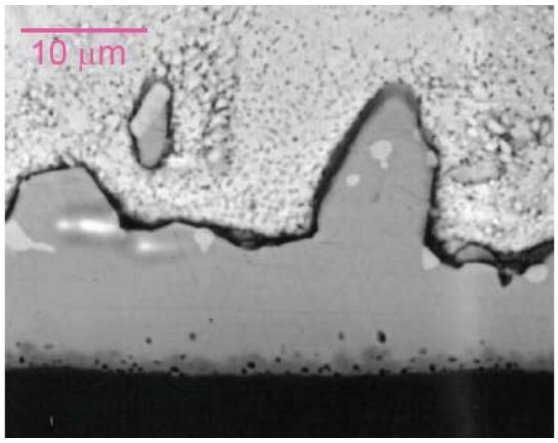
Figure 5 SEM images taken in BEI mode showing the formation of two IMC layers in the BGA Test boards assembled with SAC (a) and Sn-Pb (b) and annealed at 150°C for 40 days.

subsequently annealed at 125 °C or 150 °C for 5, 25 and 40 days. No voids were seen under any conditions., as shown in Figures 3 and 4 for SAC and Sn-Pb, respectively.

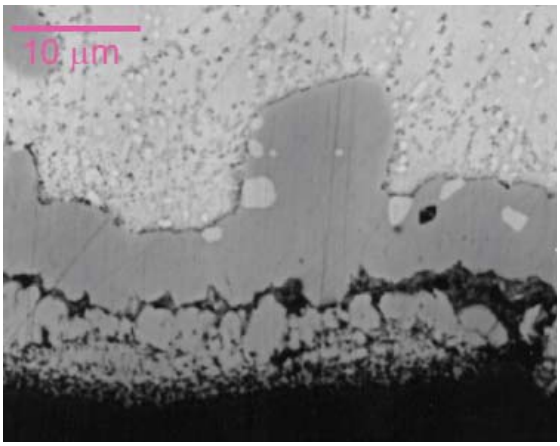
Complementary annealing experiments were performed using standard BGA test boards and components assembled with Sn-3.0Ag-0.5Cu (wt%) lead-free solder or SnPb eutectic solder (37 wt% Pb). A small volume fraction of voids was observed in all annealed samples, as seen for two examples in Figure 5. The void volume appeared to be constant with time for the three annealing times and similar for the two solders.

2.3 Electrolyte Effects on Void Formation in Solder Joints

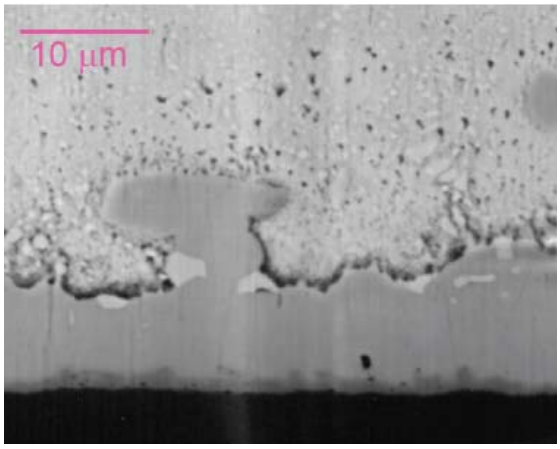
What we believe is the correct explanation for void formation between electroplated copper and Sn-containing solders can be found at least qualitatively



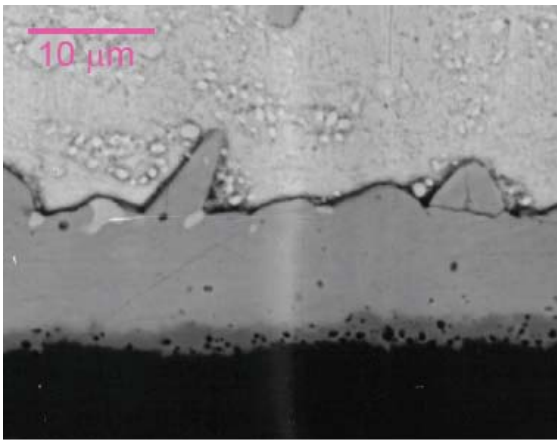
Copper A



Copper C



Copper B



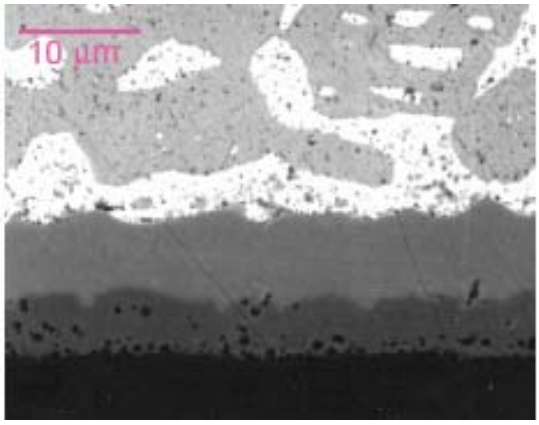
Copper D

Figure 6 Interfacial reaction and porosity formation for Sn-Ag solder on copper plated under four conditions after annealing for 160°C for 30 days: (Copper A) Surfactant A + Brightener 1, (Copper B) Surfactant A + Brightener 2; (Copper C) Surfactant A + no Brightener; (Copper D) Surfactant B + no Brightener (Figure from unpublished research of Felton, et al., 1997 [13])

from the unpublished work on Felton, Pan, et al. [13] In 1996 they noted voids forming at the interface between Sn-Ag eutectic solder and electroplated copper. They postulated that the voids formed as a result of plating bath additives being entrapped in the copper plating , and predicted that the severity of voiding depending on the bath additives, including brighteners, surfactants, leveling agents, "ductility promoting" agents, and other ingredients in the bath. Their experimental results are shown in Figure 6 (annealed with Sn-Ag eutectic) and Figure 7 (annealed with Sn-Pb eutectic) for electrodeposited copper from four different compositions of a LeaRonal acid copper electrolyte listed in the figure caption. The variability in void formation with electrolyte composition was almost as extreme as seen by Borgeson [14, 15], with the extent of voiding ranging from (least to most): B<A<D<C.

These results suggest that impurities incorporated during electrodeposition control whether voids can form. To control impurity incorporation, and therefore, void formation, the following questions should be answered:

(1) Under what conditions are impurities incorporated ?
(2) What impurities are being incorporated?
(3) Where are they located in the copper?
(4) What are the mechanisms by which the voids form during annealing and under what conditions? This has several sub-questions, including, Do the voids form when impurities are released from the copper during intermetallic formation or do the voids form when desorbed impurities transported to the Cu-Cu_3Sn interface via grain boundary diffusion during annealing?



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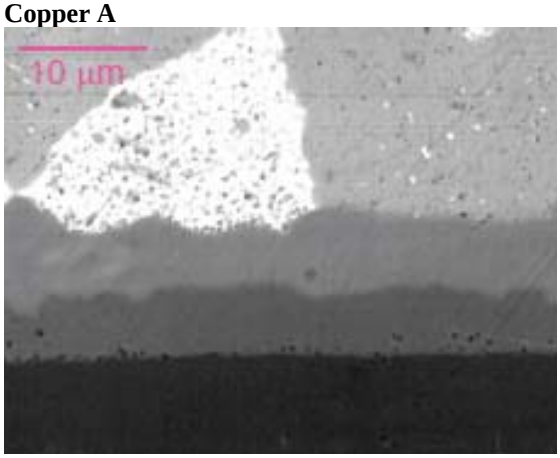
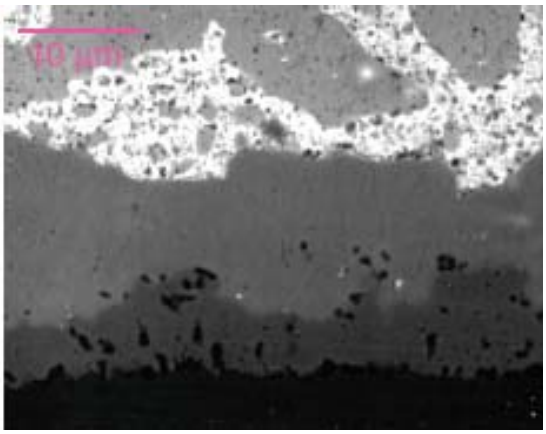
Copper A



Copper B



Copper C

Copper D

Figure 7 Interfacial reaction and porosity formation for Sn-Pb eutectic solder on copper plated under four conditions after annealing for 160°C for 30 days: (Condition A) Surfactant A + Brightener 1, (Condition B) Surfactant A + Brightener 2; (Condition C) Surfactant A + no Brightener; (Condition D) Surfactant B + no Brightener (Figure from unpublished research of Felton, et al., 1997 [13])

The final question is whether the voids, under some conditions, influence drop/shock behavior in either SAC or Sn-Pb joints.

2.4 Extensive Literature on Impurity Incorporation during Copper Electrodeposition

The answer to the first two questions can be partially answered from the scientific electrodeposition literature: it is well known in the semiconductor packaging world that impurities can be incorporated into elecrodeposited copper under a wide range of conditions. The development by IBM and worldwide implementation of electrodeposited copper as on-chip interconnects have led to an extensive body of knowledge on impurity incorporation during copper electrodeposition and their subsequent effect on the electrodeposition "superfill" or "bottom-up" filling process, grain growth, and impurity desorption from the solid electrodeposited copper. [21-27] The amount and type of impurities are functions of the electrolyte composition, bath aging (particularly associated with breakdown of the brightener with time), and plating current. [22] In addition, in electrolytes specifically design for filling high-aspect-ratio on-chip vias, more impurity incorporation has been observed when the "curvature-enhanced accelerator coverage mechanism "(CEAC) that leads to superfilling is active.[25] The impurities may include hydrogen, sulfur, oxygen, - chloride, carbon, [22, 25] and the polymeric additives themselves. Brongersma et al determined that significant desorption of carbon-related species occurs at approximately 100°C, with the desorption accompanied by a relaxation of the compressive stresses generated during deposition. [22]

3. CONCLUSIONS AND NEXT STEPS

During high temperature annealing of electrodeposited copper with Sn-containing solder, void formation is most likely determined by the presence of impurities incorporated into the copper during the electrodeposition process. As the copper

is consumed by intermetallic formation, the incorporated impurities are released at the Cu-Cu_3Sn interface, becoming free to form gas-filled pockets by a variety of mechanisms. Given the known diffusion and desorption of impurities from electrodeposited copper via grain boundary diffusion at these temperatures, this may also contribute to void formation. Additional research is necessary to answer the questions raised here, with one of the most significant being the conditions under which voids affect shock/drop performance.

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We would like to thank Bill Boettinger and Gery Stafford of the National Institute of Standards and Technology for stimulating and useful conversations. and Tsung-Yu Pan of Ford Motor Company and Larry Felton of Evergreen Solar for sharing their unpublished data and insights on the subject .

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